**Digital Design and Computer Organisation Laboratory**

**UE22CS251A**

**3rd Semester, Academic Year 2023**

Date: 10-08-2023

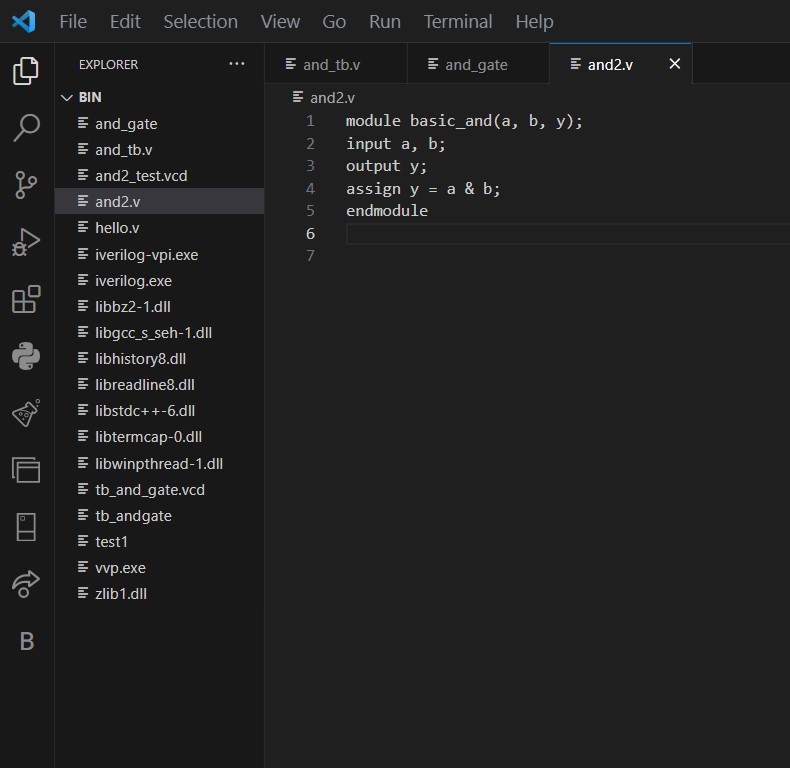
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| Name: Gurram Shreya | SRN: PES2UG22CS209 | Section: D |

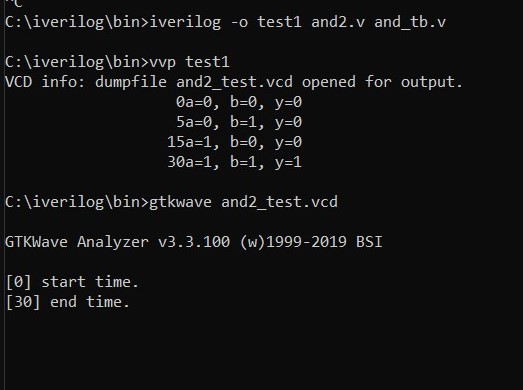
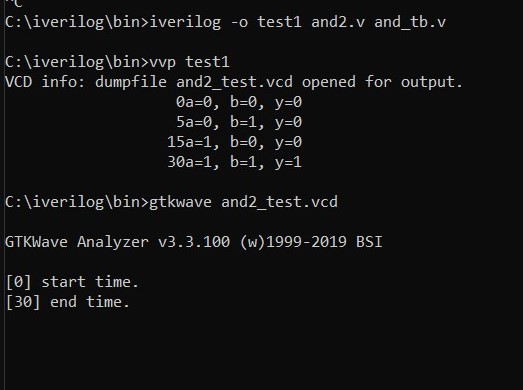
Week#\_\_\_\_1\_\_\_\_\_\_\_ Program Number: \_\_\_\_1\_\_\_

TITLE:

**WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT AND GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE**

1. Verilog Code Screenshot



1. Verilog VVP Output Screen Shot 
2. GTKWAVE Screenshot 
3. Output Table to be completed and included

|  |  |  |
| --- | --- | --- |
| a | b | y |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

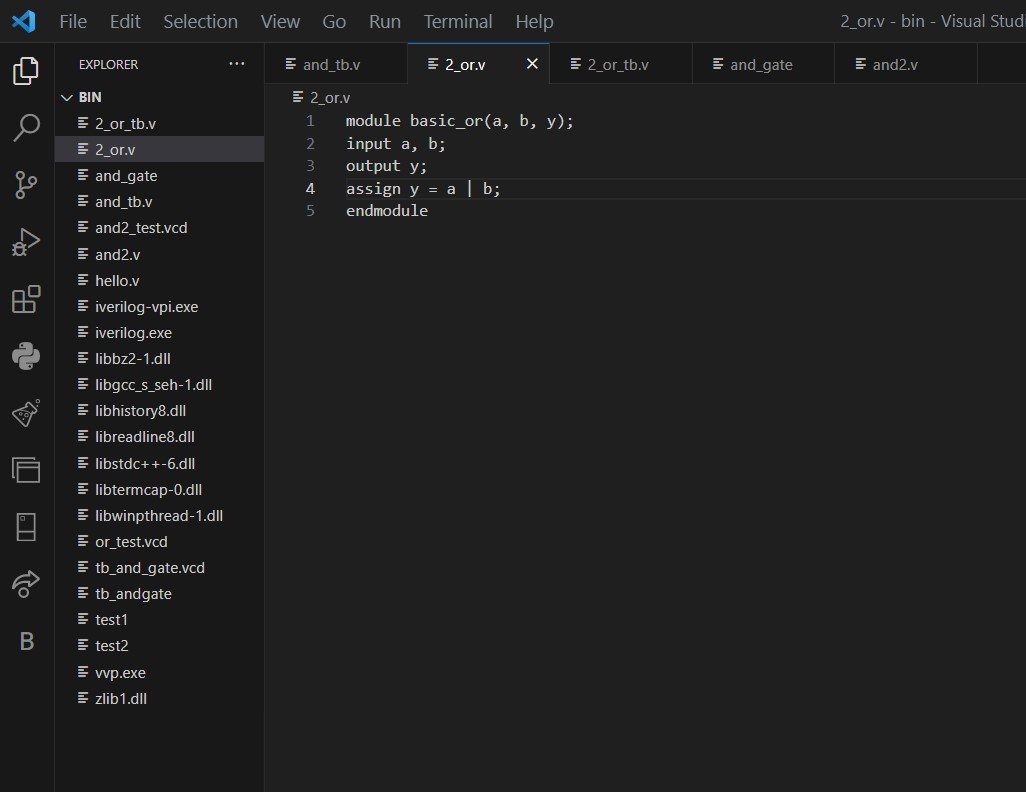
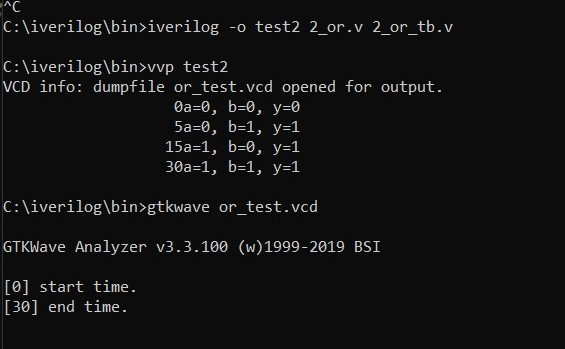
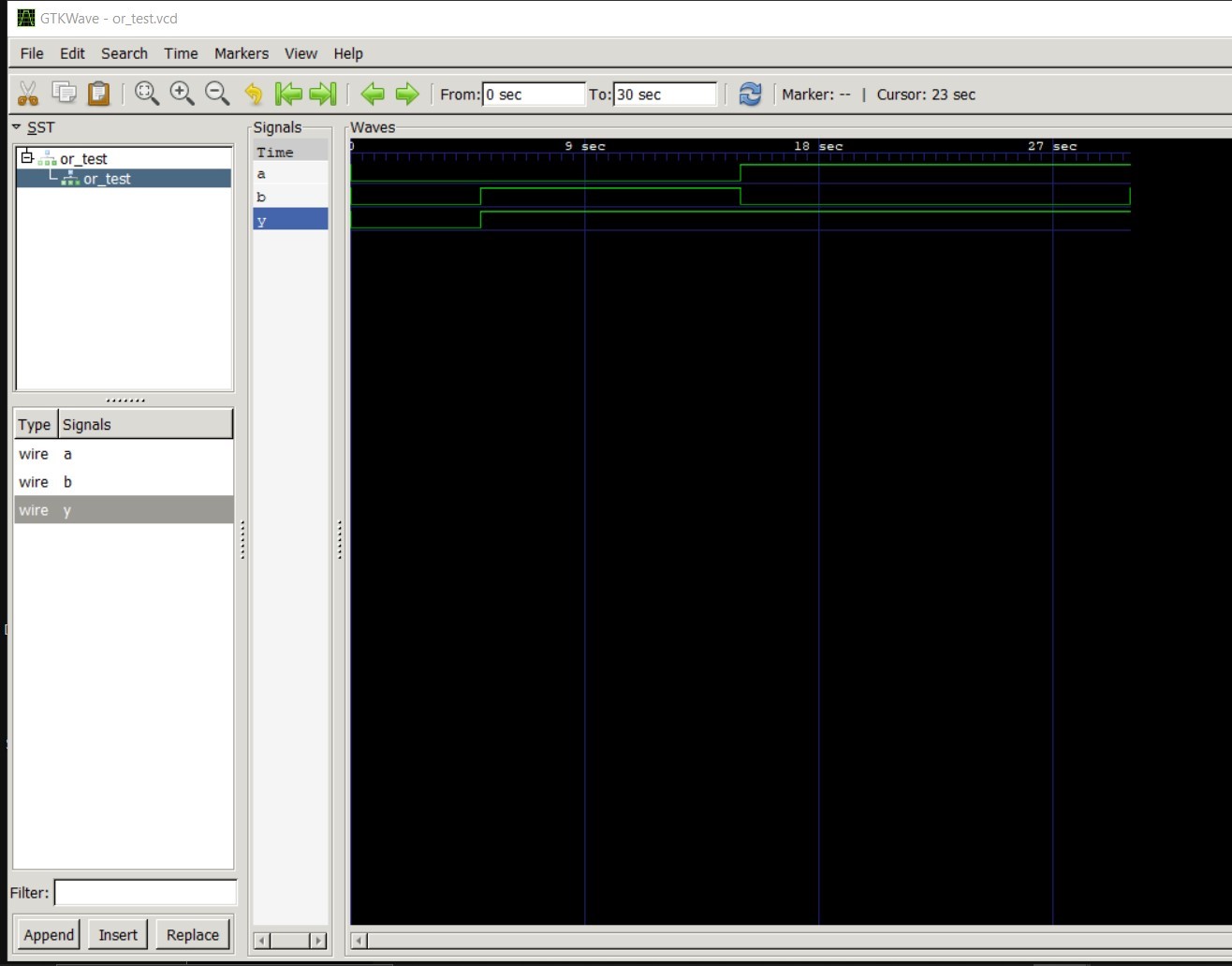
Date: 10-08-2023

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| Name: Gurram Shreya | SRN: PES2UG22CS209 | Section: D |

Week#\_\_\_\_1\_\_\_\_\_\_\_ Program Number: \_\_\_\_2\_\_\_

TITLE :

**WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT OR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE OR GATE TRUTH TABLE**

1. Verilog Code Screenshot 
2. Verilog VVP Output Screen Shot 
3. GTKWAVE Screenshot 
4. Output Table to be completed and included

|  |  |  |
| --- | --- | --- |
| a | b | y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

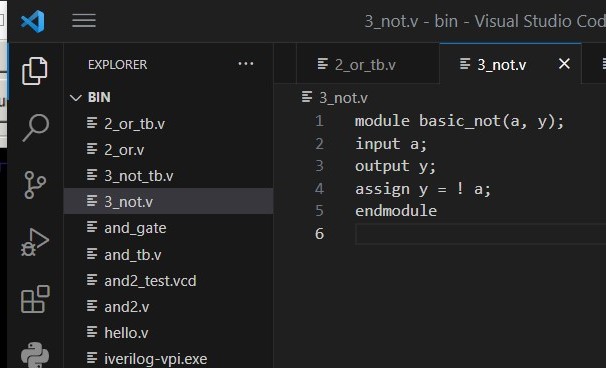
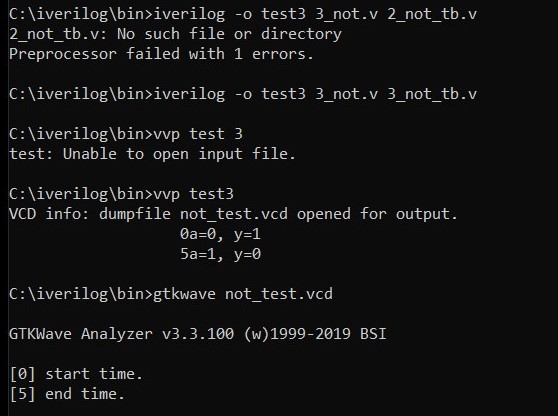
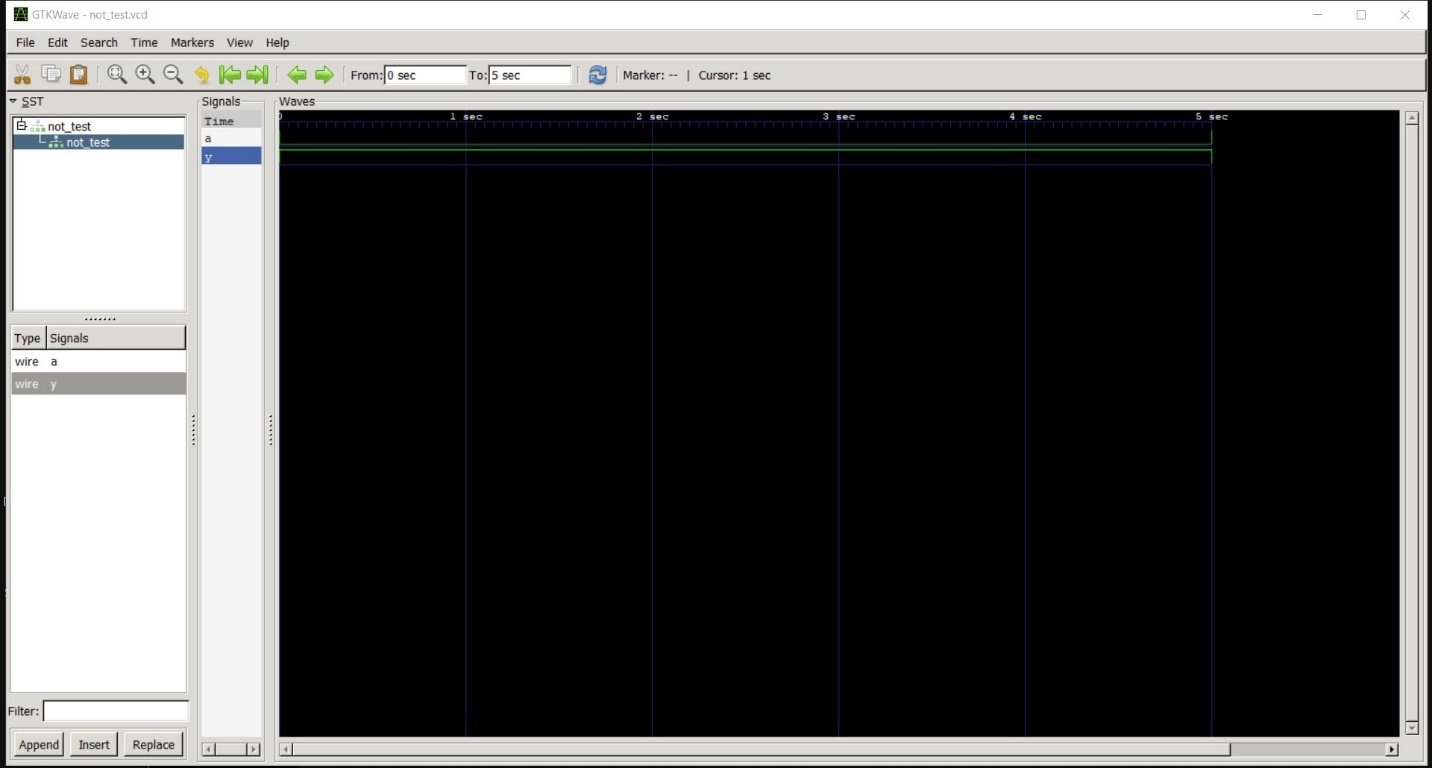
Date: 10-08-2023

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| Name: Gurram Shreya | SRN: PES2UG22CS209 | Section: D |

Week#\_\_\_\_1\_\_\_\_\_\_\_ Program Number: \_\_\_\_3\_\_\_

TITLE:

**WRITE A VERILOG PROGRAM TO MODEL A NOT GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NOT GATE TRUTH TABLE**

1. Verilog Code Screenshot 
2. Verilog VVP Output Screen Shot 
3. GTKWAVE Screenshot 
4. Output Table to be completed and included

|  |  |
| --- | --- |
| a | y |
| 0 | 1 |
| 1 | 0 |

Date: 10-08-2023

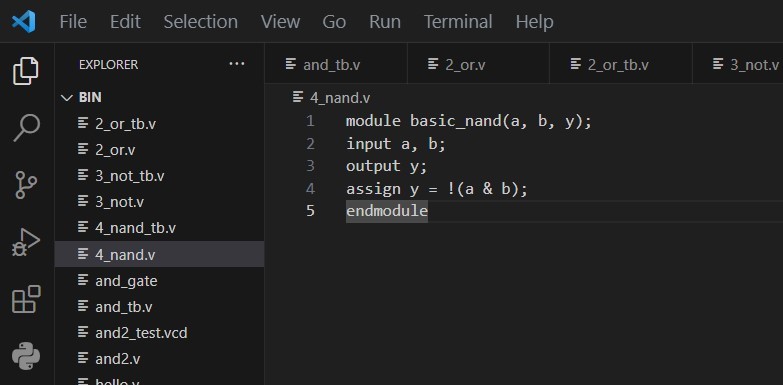
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| --- | --- | --- |
| Name: Gurram Shreya | SRN: PES2UG22CS209 | Section: D |

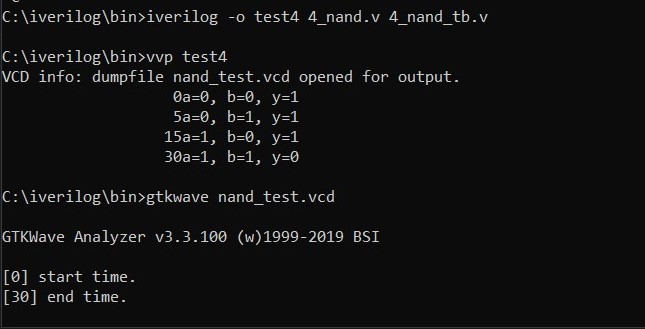
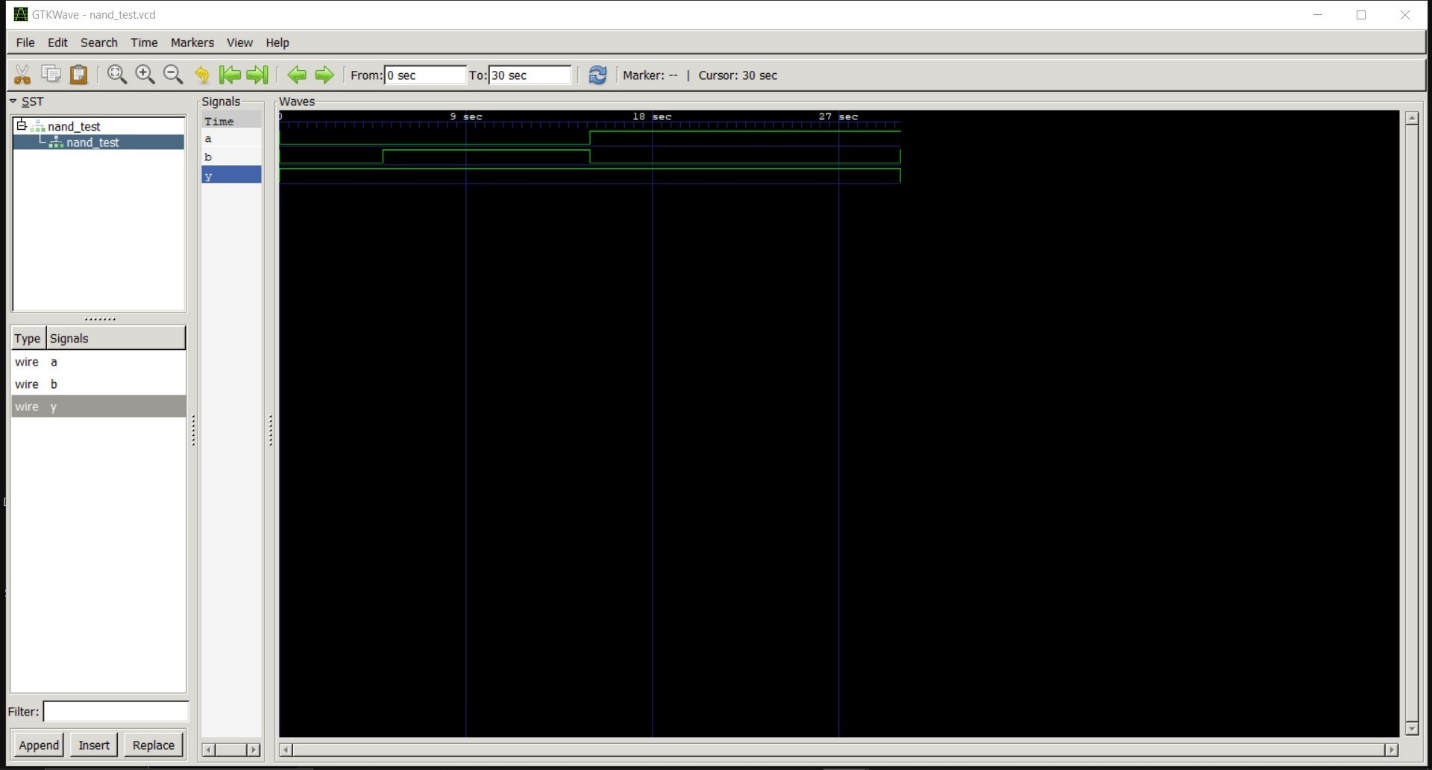
Week#\_\_\_\_1\_\_\_\_\_\_\_ Program Number: \_\_\_\_4\_\_\_

TITLE :

**WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT NAND GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NAND GATE TRUTH TABLE**

1. Verilog Code Screenshot



1. Verilog VVP Output Screen Shot 
2. GTKWAVE Screenshot 
3. Output Table to be completed and included

|  |  |  |
| --- | --- | --- |
| a | b | y |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

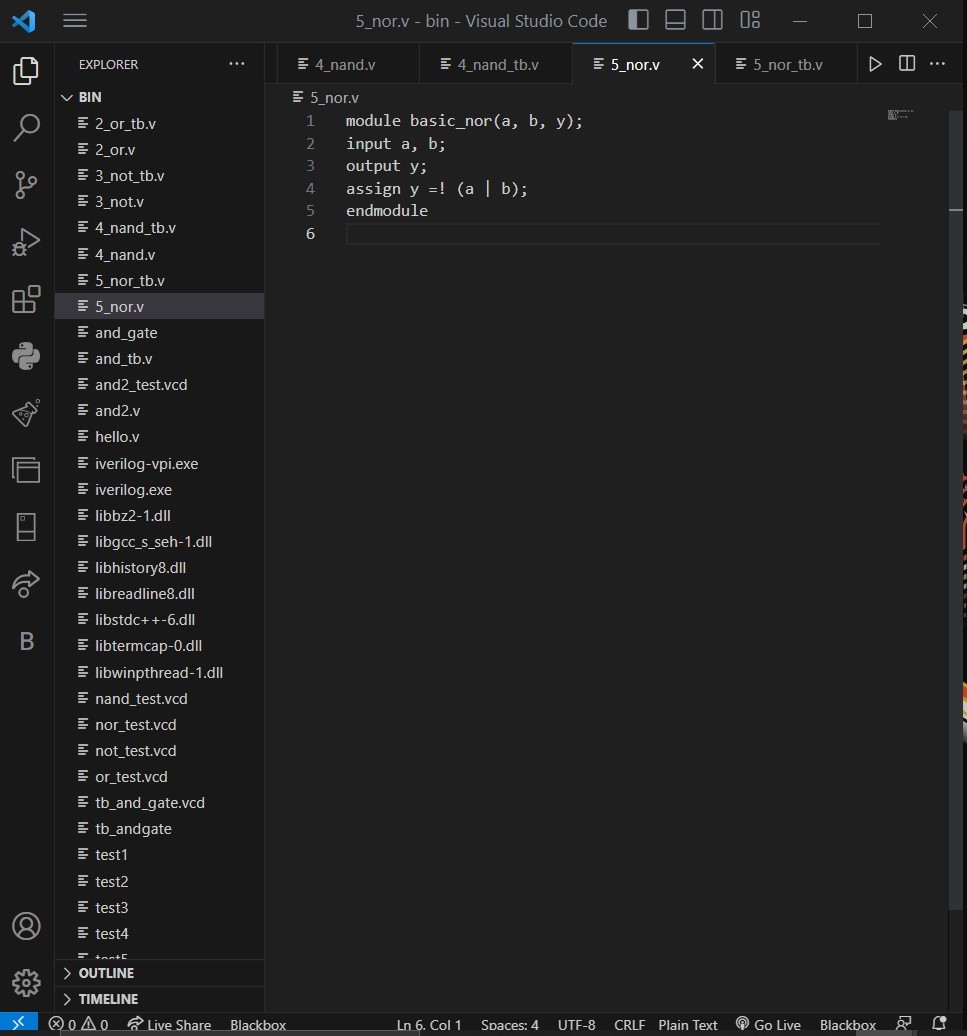
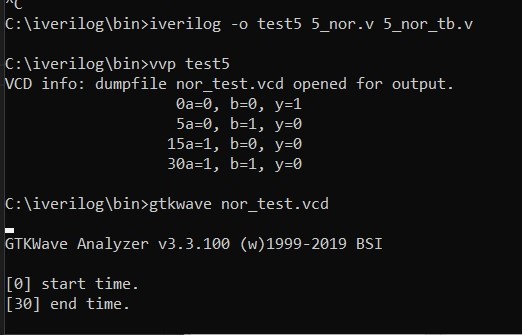
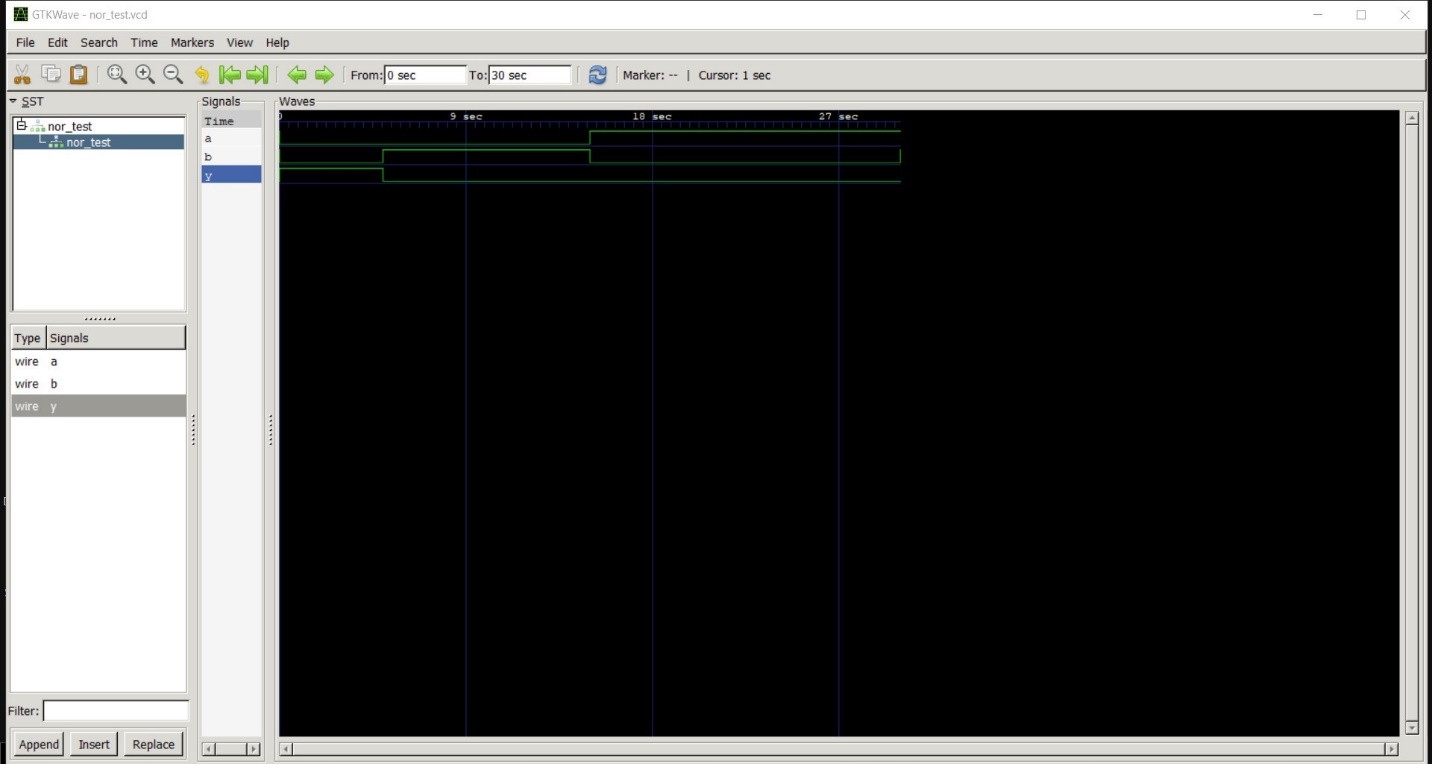
Date: 10-08-2023

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| Name: Gurram Shreya | SRN: PES2UG22CS209 | Section: D |

Week#\_\_\_\_1\_\_\_\_\_\_\_ Program Number: \_\_\_\_5\_\_\_

TITLE:

**WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT NOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NOR GATE TRUTH TABLE**

1. Verilog Code Screenshot 
2. Verilog VVP Output Screen Shot 
3. GTKWAVE Screenshot 
4. Output Table to be completed and included

|  |  |  |
| --- | --- | --- |
| a | b | y |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

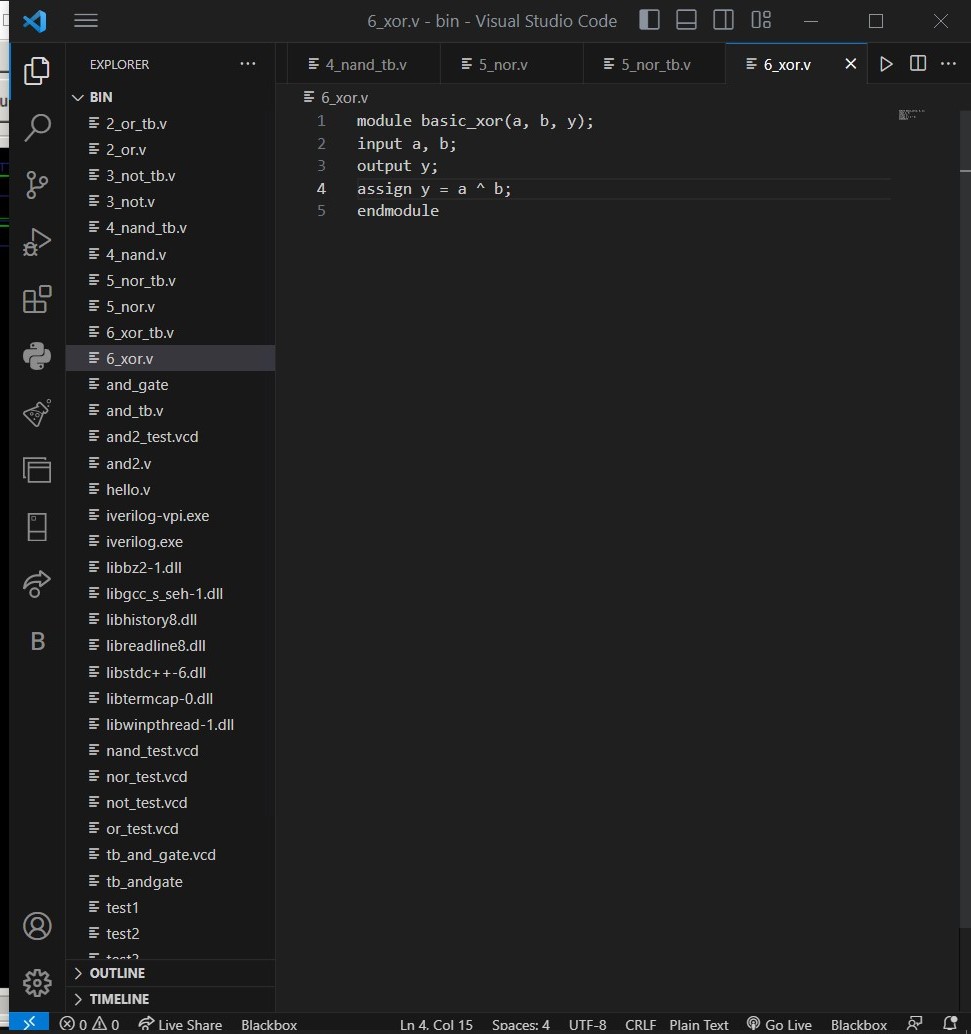
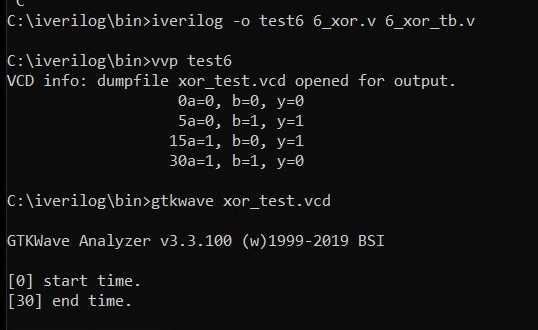
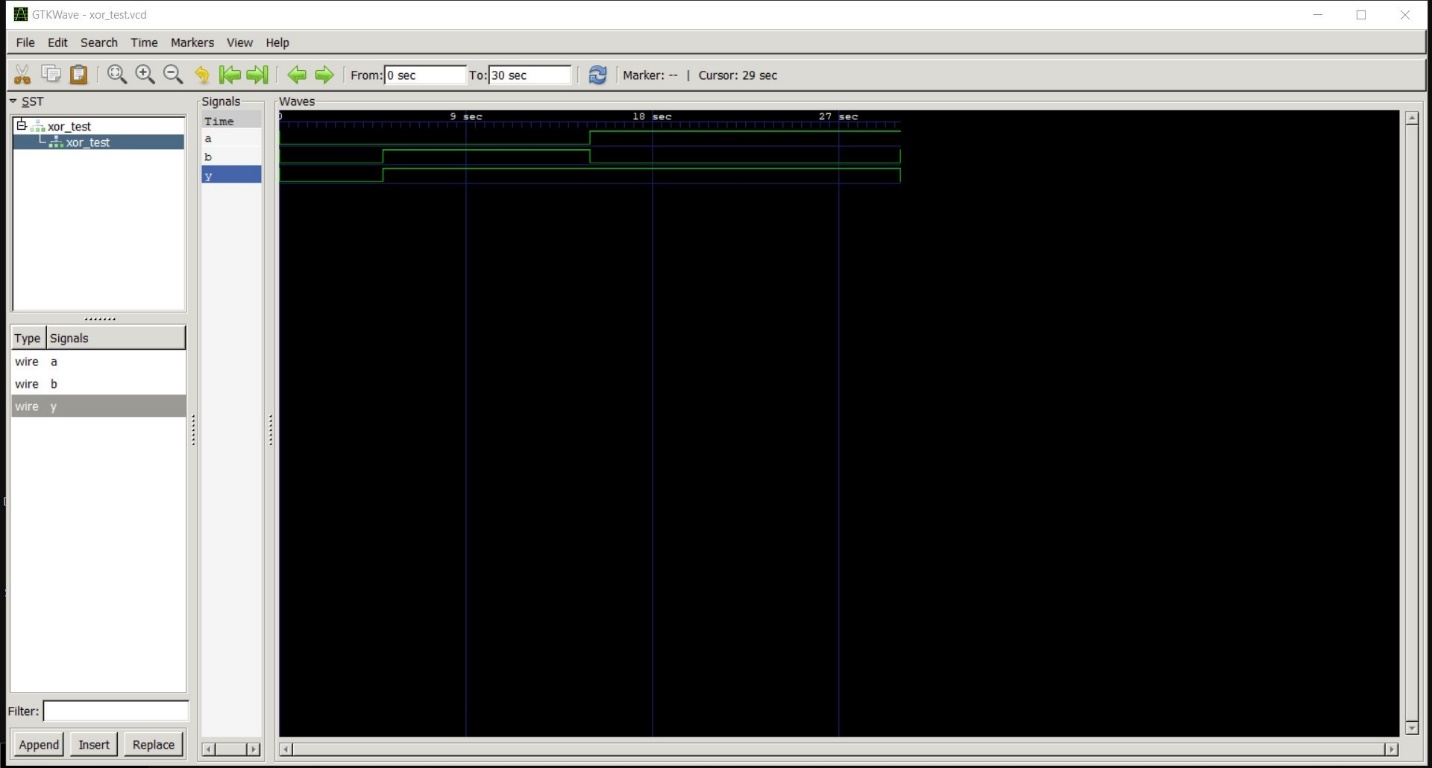
Date: 10-08-2023

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| Name: Gurram Shreya | SRN: PES2UG22CS209 | Section: D |

Week#\_\_\_\_1\_\_\_\_\_\_\_ Program Number: \_\_\_\_6\_\_

TITLE:

**WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT XOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE**

1. Verilog Code Screenshot 
2. Verilog VVP Output Screen Shot 
3. GTKWAVE Screenshot 
4. Output Table to be completed and included

|  |  |  |
| --- | --- | --- |
| a | b | y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

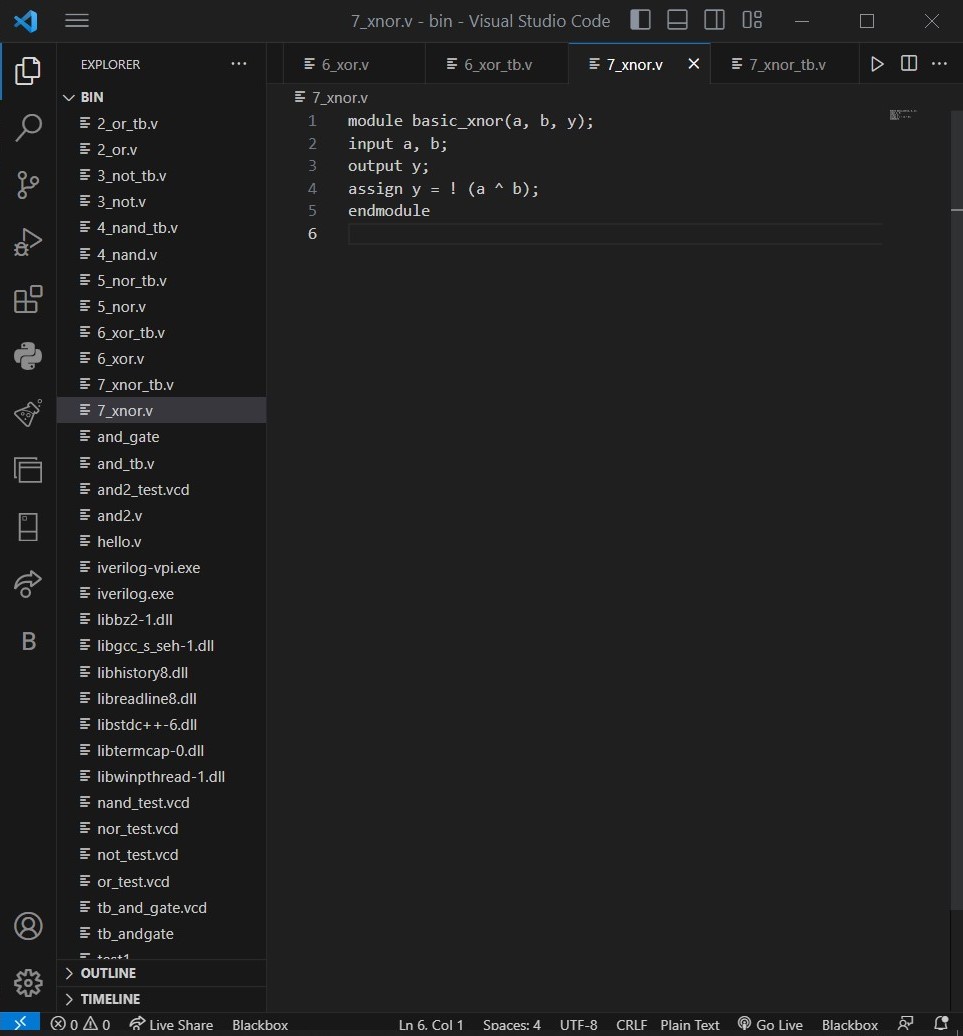
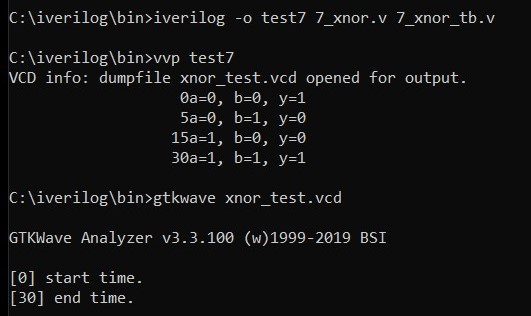
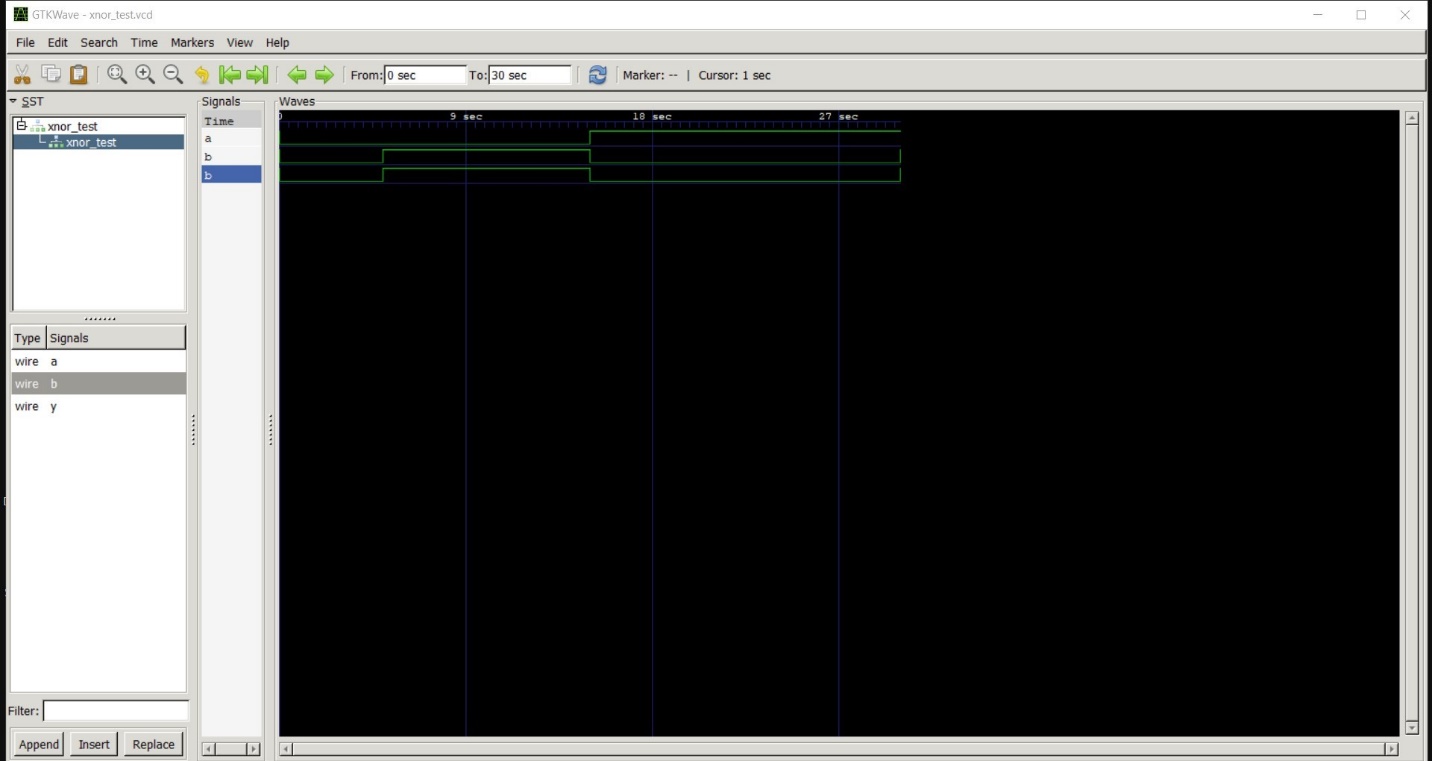
Date: 10-08-2023

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| --- | --- | --- |
| Name: Gurram Shreya | SRN: PES2UG22CS209 | Section: D |

Week#\_\_\_\_1\_\_\_\_\_\_\_ Program Number: \_\_\_\_7\_\_\_

TITLE :

**WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT XNOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE**

1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot 
3. GTKWAVE Screenshot
4. Output Table to be completed and included

|  |  |  |
| --- | --- | --- |
| a | b | y |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Disclaimer:**

* The programs and output submitted is duly written, verified and executed by me.
* I have not copied from any of my peers nor from the external resource such as internet.
* If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

Name: Gurram Shreya

SRN: PES2UG22CS209

Section: D

Date: 10-08-2023